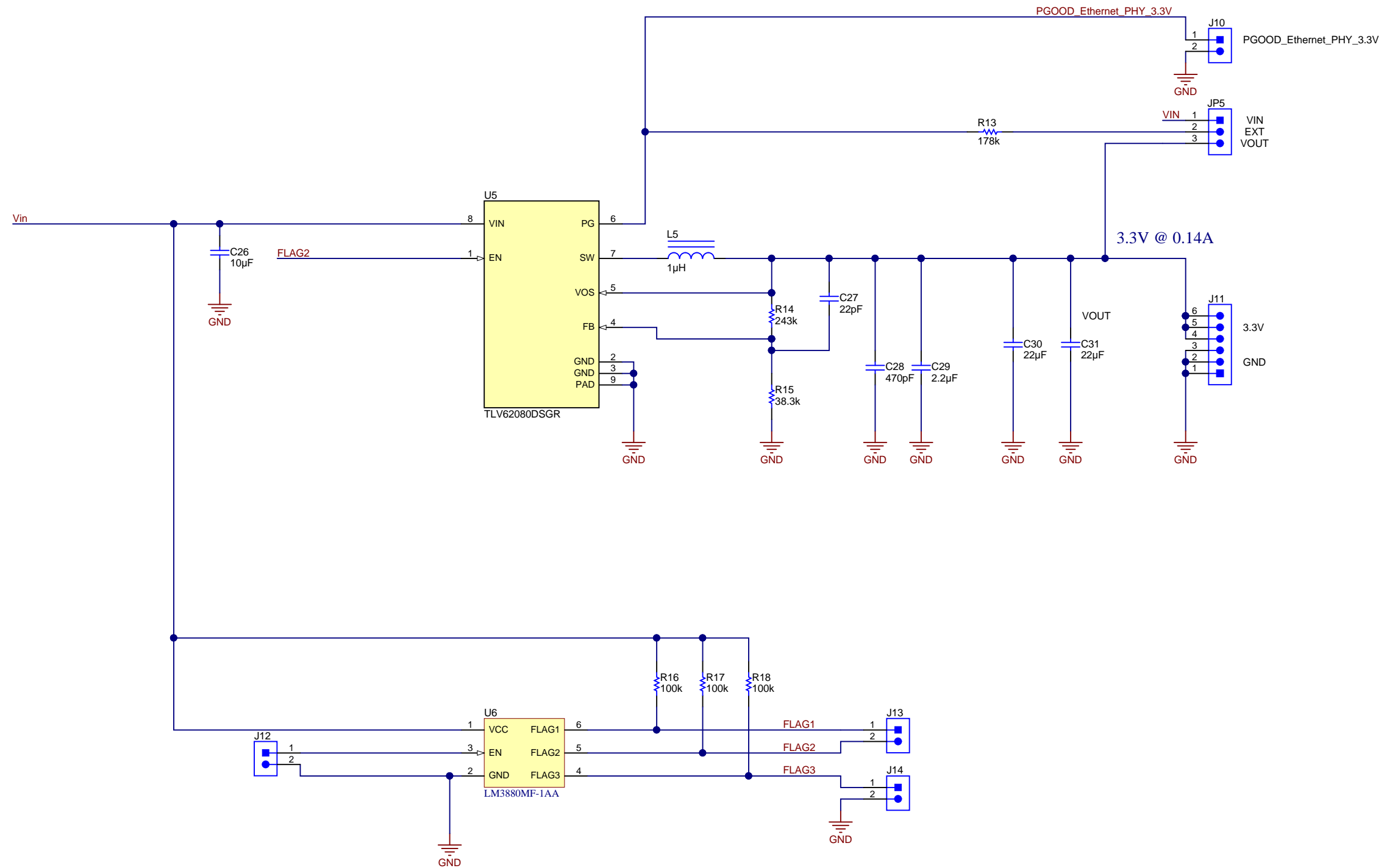



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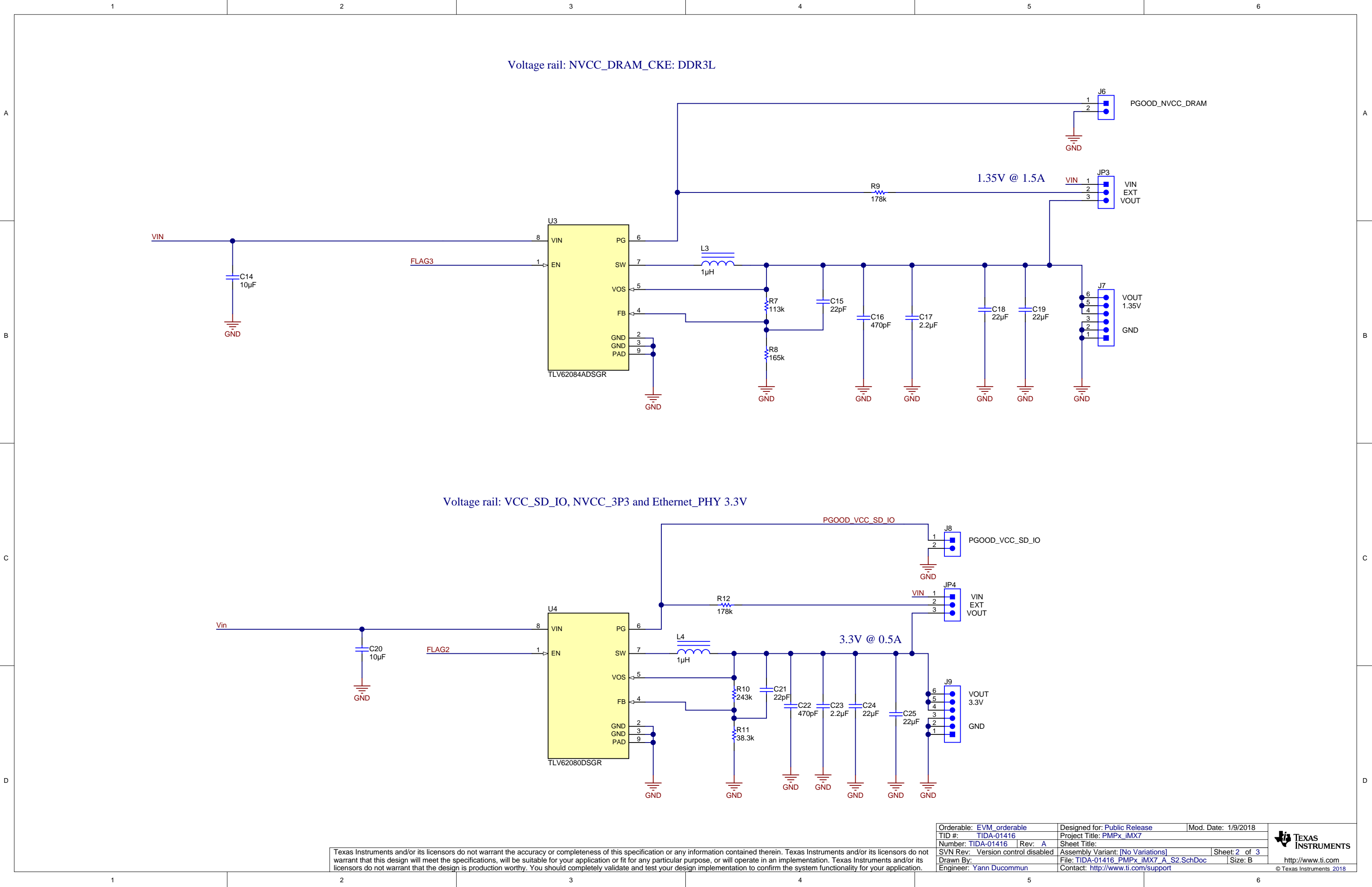
Orderable: <a href="#">EVM_orderable</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 1/9/2018
TID #: <a href="#">TIDA-01416</a>	Project Title: <a href="#">PMPx_iMX7</a>	
Number: <a href="#">TIDA-01416</a>	Rev: <a href="#">A</a>	Sheet Title:
SVN Rev: <a href="#">Version control disabled</a>	Assembly Variant: <a href="#">[No Variations]</a>	Sheet: <a href="#">1</a> of <a href="#">2</a>
Drawn By: <a href="#">Fred Illguth</a>	File: <a href="#">TIDA-01416_PMPx_iMX7_A_S1.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">Yann Ducommun</a>	Contact: <a href="#">http://www.ti.com/support</a>	

Voltage rail: Ethernet PHY 3.3V



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Number: <a href="#">TIDA-01416</a>	Rev: <a href="#">A</a>	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: <a href="#">[No Variations]</a>	Sheet: <a href="#">2</a> of <a href="#">3</a>	
Drawn By:	File: <a href="#">TIDA-01416_PMPx_iMX7_A_S3.SchDoc</a>	Size: B	
Engineer: <a href="#">Yann Ducommun</a>			<a href="http://www.ti.com">http://www.ti.com</a> Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>



Voltage rail: NVCC\_DRAM\_CKE: DDR3L

Voltage rail: VCC\_SD\_IO, NVCC\_3P3 and Ethernet\_PHY 3.3V

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TID #: <a href="#">TIDA-01416</a>	Project Title: <a href="#">PMPx_iMX7</a>	
Number: <a href="#">TIDA-01416</a>	Rev: <a href="#">A</a>	Sheet Title:
SVN Rev: <a href="#">Version control disabled</a>	Assembly Variant: <a href="#">[No Variations]</a>	Sheet: <a href="#">2</a> of <a href="#">3</a>
Drawn By:	File: <a href="#">TIDA-01416_PMPx_iMX7_A_S2.SchDoc</a>	Size: <a href="#">B</a>
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